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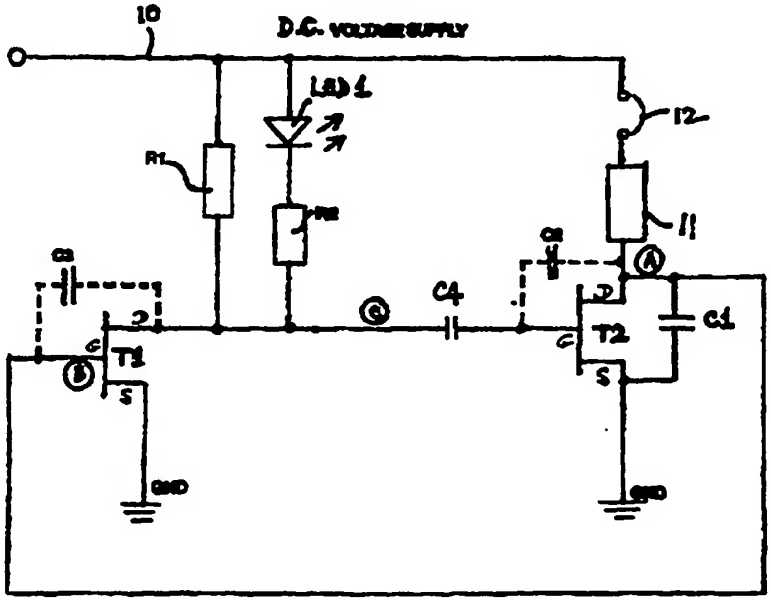
(54) Title: POWER CUT-OFF DEVICE



(57) Abstract

A power cut-off device comprises first and second electronic switching devices (FETs T2 and T1) which are cross-coupled so that when one switching device is on the other is off and vice versa, and a load (11) to be protected is connectable in series with the first switching device (FET T2). If the current through the first switching device (FET T2) exceeds a certain value, caused for example by a short circuit at the load, the second switching device (FET T1) is turned on to turn the first switching device off.

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Description

Power Cut-Off Device

Technical Field

This invention relates to a power cut-off device.

Disclosure of the Invention

According to the invention there is provided a power cut-off device comprising first and second electronic switching devices which are cross-coupled so that when one switching device is on the other is off and vice versa, wherein a load to be protected is connectable in series with the first switching device, and wherein if when the first switching device is on the current therethrough exceeds a certain value the second switching device is turned on to turn the first switching device off.

Brief Description of the Drawings

Figure 1 is a circuit diagram of a DC power cut-off device according to a first embodiment of the invention,

Figure 2 is a circuit diagram of an AC power cut-off device according to a second embodiment of the invention,

Figure 3 is a circuit diagram of a DC power cut-off device according to a third embodiment of the invention, and

Figure 4 is a circuit diagram of a DC power cut-off device according to a fourth embodiment of the invention.

Description of the Preferred Embodiments

Embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings.

The device according to figure 1 comprises a pair of field effect transistors (FETs) T1 and T2 which are cross-coupled so that the drain of each is connected to the gate of the other. FET T1 and FET T2 should have identical electrical characteristics as far as possible. The FET T1 is connected in series with a resistor R1 between a DC voltage supply 10 and ground, and the FET T2 is connected in series with a resistive load 11 to be protected, also between the DC voltage supply 10 and ground.

A capacitor C1 is connected across the source and drain of the FET T2 (at this the point ignore the capacitors C2 and C3) and a fusible link 12 is connected in series with the load 11. A light emitting diode LED 1 and series-connected resistor R2 are connected in parallel with the resistor R1.

In this embodiment the DC voltage supply 10 is 12 volts and the components have the following values:

R1: 420 ohms

R2: 400 ohms

C1: 100 nanofarads

FETs T1 and T2: Beta = 0.42

When power is switched on the FET T2 is turned on by the DC voltage applied to the gate of FET T2 via the resistor R1. A capacitor C4 in series with the gate of FET T2 speeds up the operation of the device and ensures that FET T2 turns on while FET T1 remains off. As a result, a small current flows through the RC network comprising capacitor C1 and resistive load 11 at a rate determined by the resistance of the load 11 and the value of the capacitor C1. This causes the voltage to fall at the point A which holds the point B (the gate of FET T1) low. Thus FET T1 is held off and the point C (the gate of FET T2) is high to hold on FET T2 so that the supply 10 is applied to the load 11. This is the normal operating condition of the device, wherein the point A remains low, and thereby holds off the FET T1, all the while the FET T2 is on.

When a short circuit is applied across the resistive load 11 to simulate a fault condition, the point A rises substantially to the voltage of the DC supply 10 at a rate determined by the charge time of the capacitor C1, so that substantially the entire 10 volt supply is placed across the source and drain of the FET T2. Concurrently the current flowing through the FET T2 will increase. However, the 10 volt supply voltage across FET T2 drives the latter into saturation, so that the current through FET T2 is limited to the constant saturation current. The saturation current depends upon the power rating of the FET T2 (essentially its physical size) and its value of Beta. In the present case it is assumed that the saturation current is 5 amps.

Although the maximum current flowing through FET T2 is limited to the saturation current in the case of a fault, this situation cannot be permitted to persist. However, when the point A goes high so will the point B. This switches on the FET T1 so that the point C is pulled low which in turn switches off the FET T2 to remove power from the load 11.

A small current now flows from the DC supply 10 to ground via the FET T1 just sufficient to keep the FET T1 on, the part of this current flowing through the resistor R2 and the LED 1 being just sufficient to illuminate the LED 1 to provide an indication that a short has occurred. The value of the resistor R1 should be selected so that it can effectively switch on the FET T1 with as little power consumption as possible.

When a fault has occurred the power is switched off and the fault fixed, after which the power is switched on again to resume the normal operating condition as described above. The LED 1 and associated resistor R2 may be omitted if it is not desired to provide a visual indication of a fault.

The capacitor C1 is responsible for the device's cut-off delay, and should be chosen so as to filter out switching transients and allow for the inrush of current in motors, lamps, heaters, etc.

As mentioned above, the saturation current of the FET T2 is dependent in part upon the beta of the FET T2. The beta of FET T2 has to be carefully

chosen. If it is too high the resistance of the FET T2 in the ON state during normal operation will cause undue heat dissipation which may harm the device in the long term and in any event is inefficient. On the other hand, if the beta is too low the saturation current will be too high which may cause the device to blow. We have found that a beta in the range 0.42 - 0.48 is a compromise between these two extremes and provides satisfactory performance. We have also found that a beta below 0.37 or above 0.55 is unsatisfactory. Although the switching time of the device may be adjusted by selecting different values for the capacitor C1, the speed is ultimately limited by the operating speed of the field effect transistors FET T1 and FET T2, which is typically 15ns. However, a further increase in speed may be achieved by connecting additional capacitors C2 and C3 respectively across the drain-gate path of each FET. Also, by selecting different values for C2 and C3 one can provide different speeds for switching the device on and switching it off.

The fusible link 12 is connected in series with the load 11 as a fail-safe feature. If a fault occurs in the device the load is still protected by the fusible link. The link 12 is designed to blow at a current slightly higher than the cut-off current of the device.

Referring now to figure 2, the AC power cut-off device essentially comprises two sub-circuits similar to the circuit described above for the DC case (except that the load 11 is connected in series with both FETs T1 and T2 rather than just the FET T2), and in figure 2 the same or similar components have been given the same reference numerals as in figure 1. One sub-circuit consists of the cross-coupled FETs T1 and T2 and is responsive to positive half cycles of the AC voltage and the other sub-circuit consists of the cross-coupled FETs T1' and T2' and is responsive to the negative half cycles, as determined by diodes D1 and D2.

During positive half cycles the sub-circuit comprising FETs T1 and T2 operates substantially as described above for the DC case, the FET T2 being on and the FET T1 being off during normal operation. When there is a fault, the FET T2 turns off and the FET T1 turns on. During the negative half cycles both FETs T1 and T2 are off. In this embodiment the resistor

R1 has a large value to limit the current flowing through FET T1 when the latter is on.

Similarly, in the sub-circuit comprising FETs T1' and T2', during negative half cycles the FET T2' is on and the FET T1' is off during normal operation and when there is a fault, the FET T2' turns off and the FET T1' turns on. During the positive half cycles both FETs T1' and T2' are off.In this embodiment it is necessary that the FETs T1 and T2 be of complementary type to the FETs T1' and T2'. Hence, in this case the FETs T1 and T2 are p-channel devices whereas the FETs T1' and T2' are n-channel devices.

As in the DC embodiment, it is possible to modify the characteristics of the circuit by adding capacitors equivalent to those indicated at C2 and C3 in figure 1 across the drain-gate paths of each of the FETs in each of the two sub-circuits of figure 2. Also, analogous to figure 1, a respective resistor R2 and LED 1 may be connected in parallel with each of the resistors R1 and R1' to provide a visual indication of a fault.

Figure 3 shows a further embodiment of a DC power cut-off device which uses only two input/output pins rather than three as for figure 1. These are the pins shown at 14 and 15 by which the device is connected in series with the load 11 between the D.C. voltage supply and ground. It will be noted that the device of figure 3 is very similar to one half of the device of figure 2, in that the load 11 is connected in series with both FETs T1 and T2.

The device of figure 3 again comprises a pair of field effect transistors T1 and T2 which are cross-coupled so that the drain of each is connected to the gate of the other. The load 11 is connected directly to the drain of the FET T2 and via a variable resistor VR1 to the gate of the FET T1, and it is also connected via a large resistor R1 to the line connecting the drain of FET T1 to the gate of FET T2.

The RC time constant at the FET T2 is shorter than that at the FET T1 (because of the capacitor C5 connected across the gate-drain path of the FET T1) so that when power is switched on the FET T2 switches on before

the FET T1. Thus the drain of the FET T2 goes low which pulls the gate of the FET T1 low via the resistor R3 to prevent the FET T1 from turning on. This is the normal operating condition of the device, with the FET T2 turned on so as to complete a path to ground for current through the load 11 while the FET T1 is held off.In the case of a fault condition such as a short circuit in the load 11 the voltage at the drain of the FET T2 rises and, when it reaches the threshold voltage of the FET T1 (as established by the value of VR1), the FET T1 turns on. The drain of the FET T1 then goes low and, because the drain of the FET T1 is connected to the gate of the FET T2, the FET T2 is turned off. The RC time constant of the capacitor C5 and resistor R3 is selected to provide an appropriate turn on time for the FET T1 so that switching transients and the like do not inadvertently trigger the device.

In the embodiment of figure 3 the turn on time of the FET T2 is given by:

$$(1.1) \times R1 \times C6$$

where R1 = 10Kohms and C6 = 0.0000001uF being the capacitance of the gate oxide layer of FET T2, and the cut off time of the device in the case of a fault current is given by:

$$(1.1) \times (VR1//R3) \times C5$$

where R3 = 30Kohms and C5 = 1uF.

As before, it is possible to modify the characteristics of the circuit by adding capacitors equivalent to those indicated at C2 and C3 in figure 1 across the source-gate paths of each of the FETs T1 and T2. Also, a resistor R2 and LED 1 may be connected in parallel with the resistor R1 to provide a visual indication of a fault.

A fourth embodiment of the invention (figure 4) is similar to the circuit shown in figure 3 except that (a) the FET T1 is replaced by a bipolar NPN transistor N, (b) the variable resistance VR1 is omitted, (c) the capacitor C5 is omitted, and (d) the resistor R3 is replaced by a variable resistor

VR3. However, the circuit operates in substantially the same manner as figure 3 except that the threshold of the transistor N is determined by the value of VR3.

In all embodiments a zener diode and a resistor can be applied across the DC or AC supply so that the device can be used as an over-voltage protector that can occur in spike voltages or in fault conditions.

The field effect transistors used in the above circuits may be JFETs, MOSFETs, NMOSFETs, DMOSFETS or any other kind. The circuits can be fabricated on silicon or gallium arsenide wafers using semiconductor technology or as hybrids. It is also possible to use FETs with a silicon carbide substrate to withstand the high operating voltage, current and temperature conditions of the device.

CLAIMS

1. A power cut-off device comprising first and second electronic switching devices which are cross-coupled so that when one switching device is on the other is off and vice versa, wherein a load to be protected is connectable in series with the first switching device, and wherein if when the first switching device is on the current therethrough exceeds a certain value the second switching device is turned on to turn the first switching device off.

2. A power cut-off device as claimed in claim 1, wherein the first switching device is an FET and if the load is short circuited substantially the entire supply voltage is placed across the source and drain of the FET.

3. A power cut-off device as claimed in claim 2, wherein the FET goes into saturation when the supply voltage is placed across its source and drain so that the current through the FET is limited to its saturation current.

4. A power cut-off device as claimed in claim 3, wherein the FET has a beta of from 0.42 to 0.48.

5. A power cut-off device as claimed in any preceding claim, wherein an impedence is connected in series with the second switching device through which current flows when the second switching device is turned on.

6. A power cut-off device as claimed in claim 5, wherein the load is also connected in series with the impedence.

7. A power cut-off device as claimed in any preceding claim, wherein a device is connected in series with the second switching device to provide a visual indication when the latter is switched on.

8. A power cut-off device as claimed in any preceding claim, further including a capacitor arranged to delay the turning on of the second switching device to prevent the device triggering in response to switching transients and the like.

9. A power cut-off device for an A.C. power supply, comprising two devices as claimed in any preceding claim respectively connected to the load by oppositely directed unidirectional current devices.

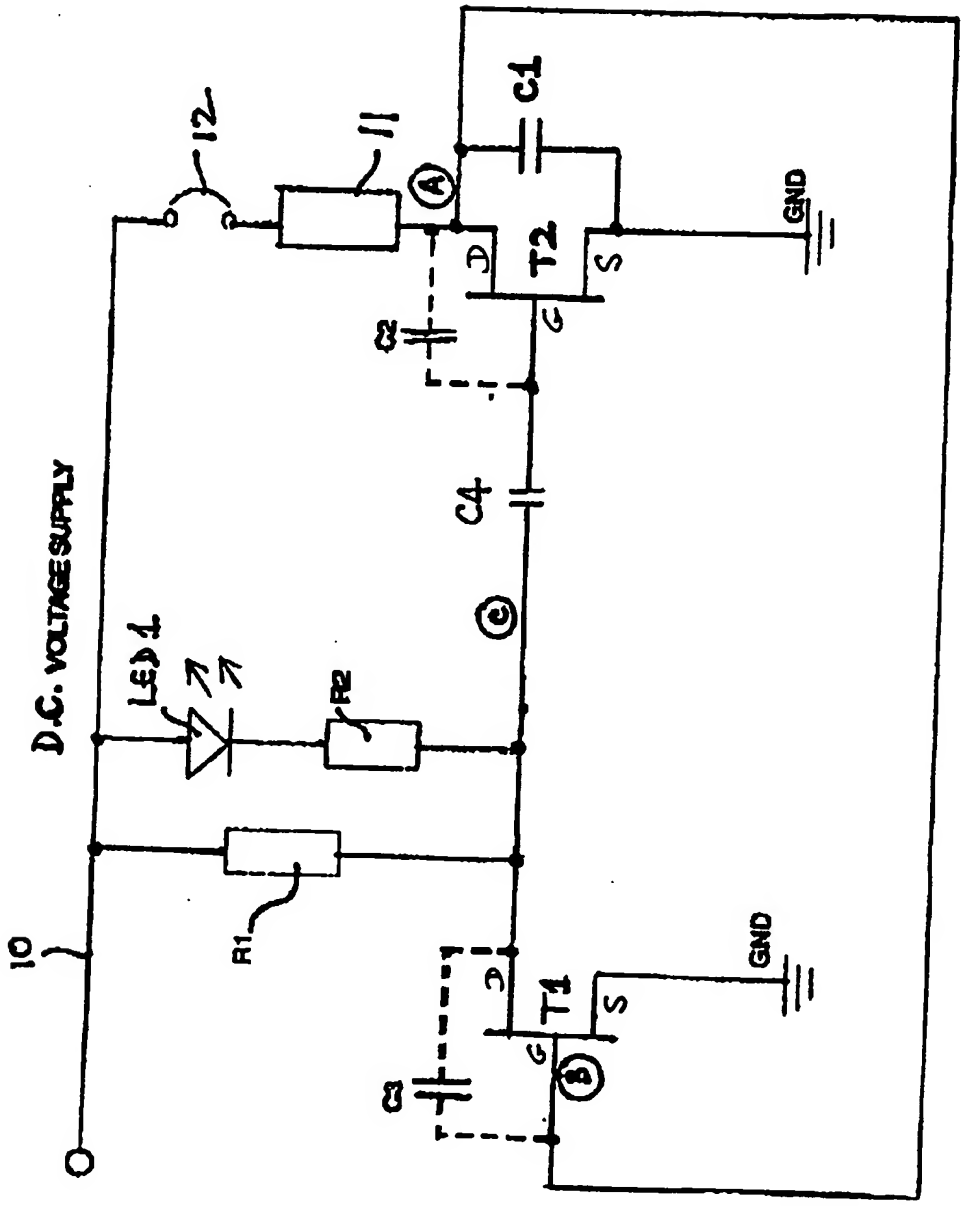

FIGURE 1.

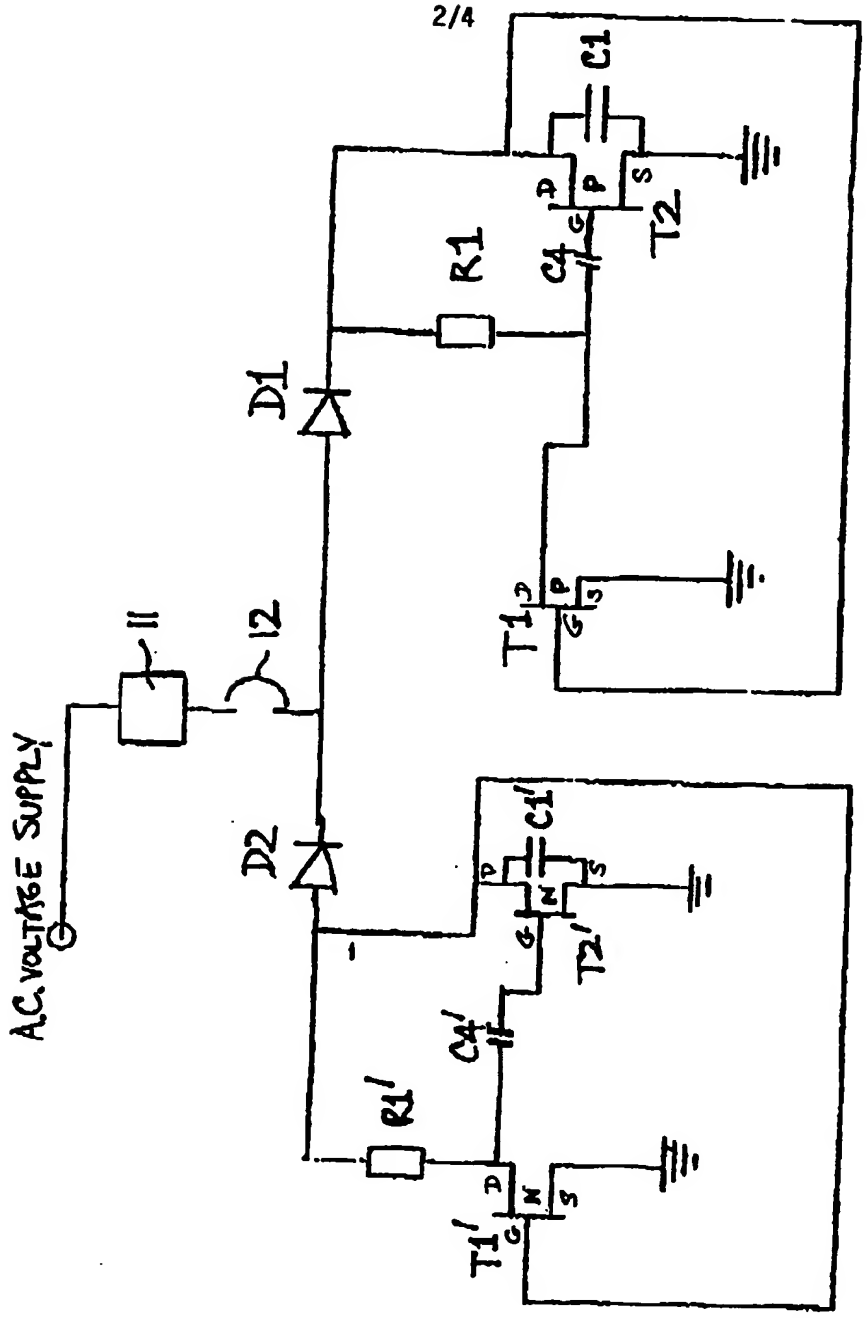
C1
P
P
S
T2
G
C4
R1
D1
T1
G
P
S
I1
I2
D2
A.C. VOLTAGE SUPPLY
C1'
D
N
S
T2'
G
C4'
R1'
T1'
D
N
S
G

FIGURE 2.

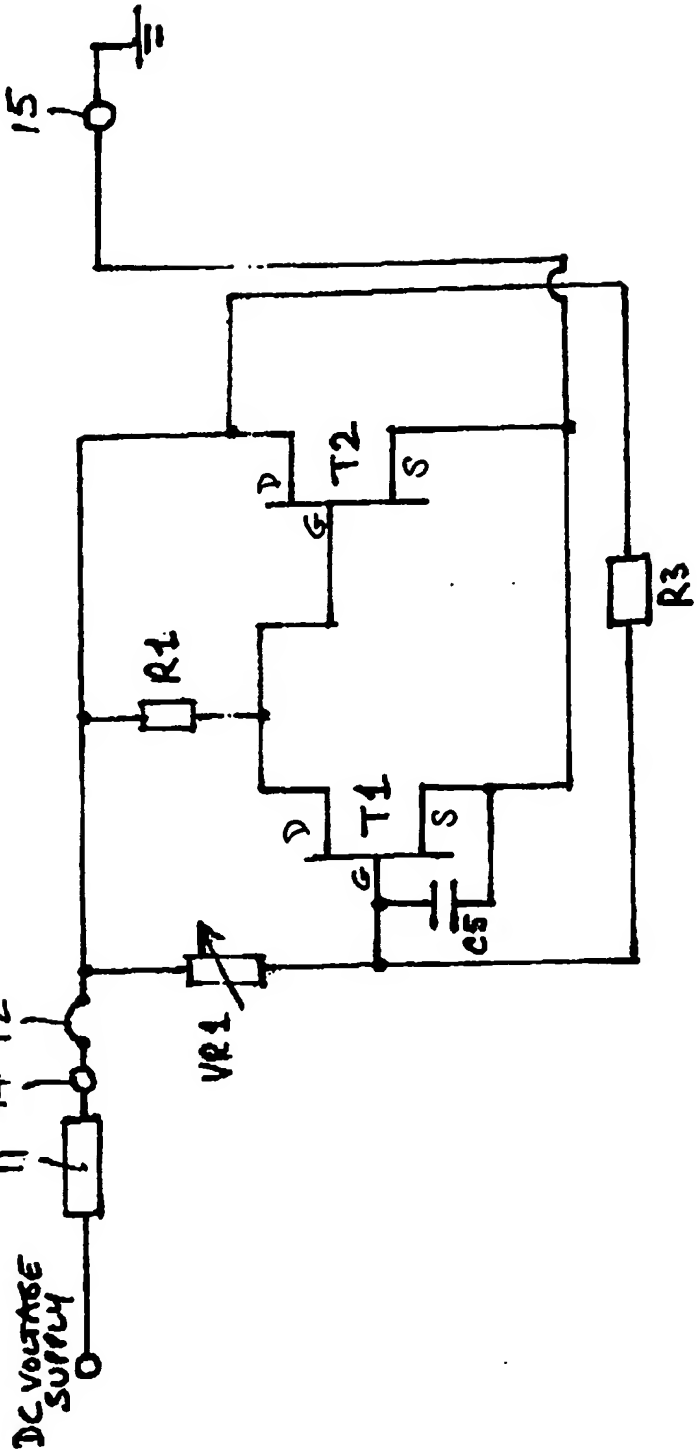

Fig 3

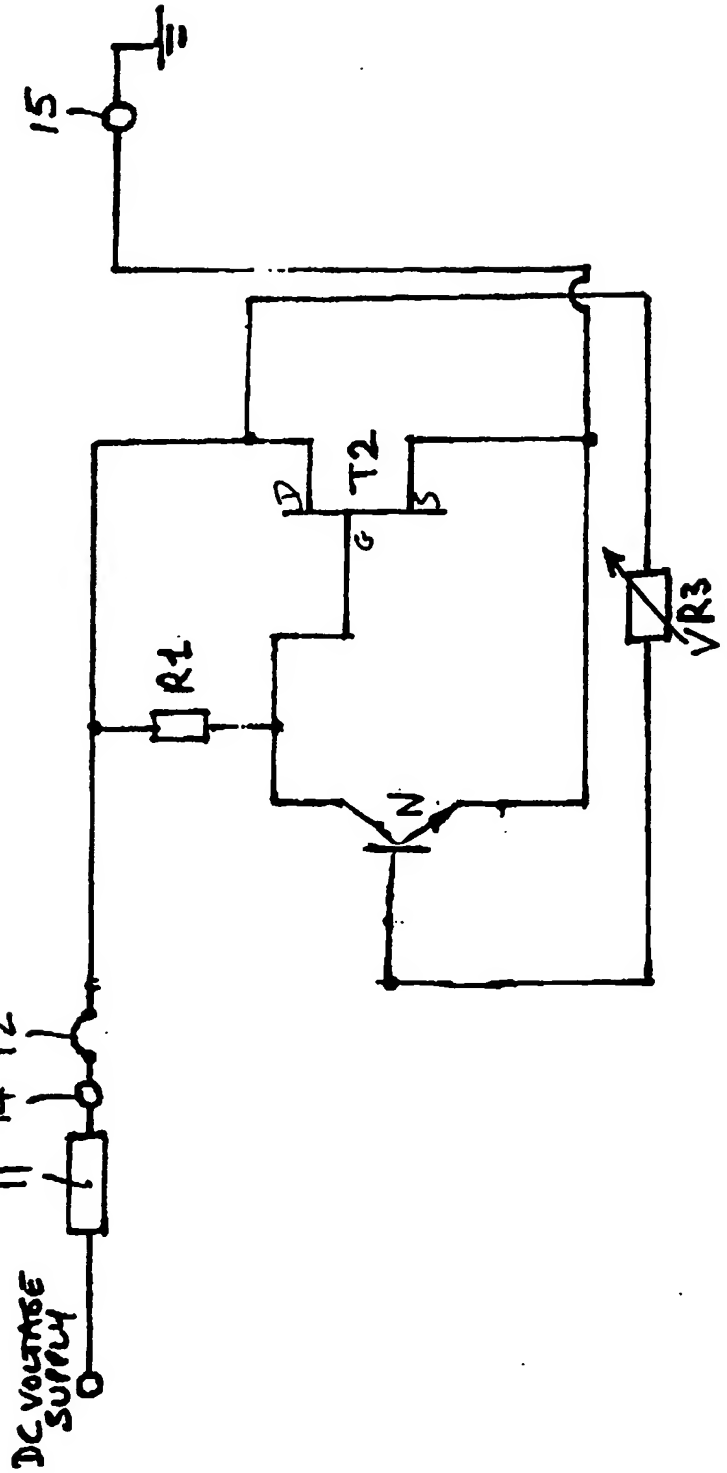

Fig 4

INTERNATIONAL SEARCH REPORT

Inter ial Application No
PCT/IE 95/00047

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H02H3/087 H03K17/082

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H02H H03K

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	DE,A,42 37 489 (BOSCH GMBH ROBERT) 11 May 1994 see column 2, line 56 - line 64; figure 1	1-3,5,8
X	EP,A,0 133 789 (BRITISH TELECOMM) 6 March 1985 see abstract	1-3
X	US,A,4 394 703 (BUTCHER JAMES S) 19 July 1983 see column 4, line 15 - line 41; figure	1,5,7,8

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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22 December 1995	10.01.96

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INTERNATIONAL SEARCH REPORT

.iformation on patent family members

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DE-A-4237489	11-05-94	WO-A-	9411947	26-05-94
		EP-A-	0620957	26-10-94
		JP-T-	7502876	23-03-95
		US-A-	5424892	13-06-95
EP-A-0133789	06-03-85	DE-A-	3473707	29-09-88
		US-A-	4686383	11-08-87
US-A-4394703	19-07-83	BE-A-	895453	15-04-83
		CA-A-	1182168	05-02-85